+30 V / ±15 V Operation 128-Position Digital Potentiometer

Preliminary Technical Data

AD7376

FEATURES

128 positions
10 kΩ, 50 kΩ, 100 kΩ
+5 V to +30 V single-supply operation
±5 V to ±15 V dual-supply operation
3-wire SPI-compatible serial interface
THD 0.006% typical
Programmable preset[1]
Power shutdown: less than 1 µA
***i*CMOS™ [4] process technology**

APPLICATIONS

High voltage DAC
Programmable power supply
Programmable gain and offset adjustment
Programmable filters, delays
Actuator control
Audio volume control
Mechanical potentiometer replacement

FUNCTIONAL BLOCK DIAGRAM

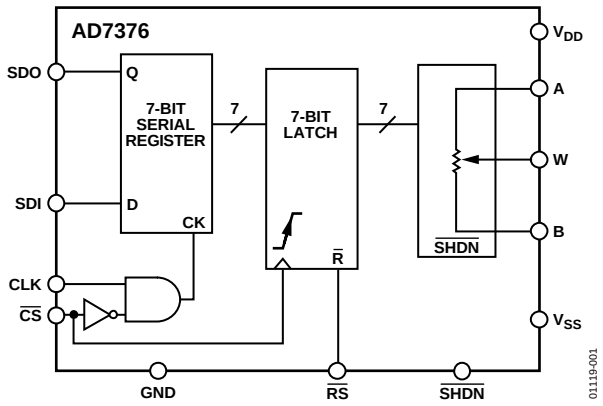

Figure 1.

GENERAL DESCRIPTION

The AD7376[2] is one of the few high voltage, high performance digital potentiometers[3] in the market at present. This device can be used as a programmable resistor or resistor divider. The AD7376 performs the same electronic adjustment function as mechanical potentiometers, variable resistors, and trimmers with enhanced resolution, solid-state reliability, and programmability. With digital rather than manual control, AD7376 provides layout flexibility and allows close-loop dynamic controllability.

The AD7376 features sleep-mode programmability in shutdown that can be used to program preset before device activation thus providing an alternative to costly EEPROM solution.

The AD7376 is available in TSSOP-14 and wide body SOIC-16 packages in 10 kΩ, 50 kΩ, and 100 kΩ options. All parts are guaranteed to operate over the –40°C to +85°C extended industrial temperature range.

[1] Assert shutdown and program the device during power up. Then deassert the shutdown to achieve the desirable preset level.
[2] Patent Number: 54952455
[3] The terms digital potentiometer and RDAC are used interchangeably.
[4] *i*CMOS™ Process Technology
For analog systems designers who need high performance ICs at higher-voltage levels, *i*CMOS is a technology platform that enables the development of analog ICs capable of 30V and operating at +/-15V supplies while allowing dramatic reductions in power consumption and package size, and increased AC and DC performance.

Rev. PrA
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REVISION HISTORY

5/05—Rev. 0 to Rev. A

Revision 0: Initial Version

AD7376—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—10 kΩ VERSION

V_{DD}/V_{SS} = ±15 V ± 10%, $V_A = +V_{DD}$, $V_B = V_{SS}/0$ V, −40°C < T_A < +85°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A = NC, V_{DD}/V_{SS} = ±15 V	−1	±0.5	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A = NC, V_{DD}/V_{SS} = ±15 V	−1	±0.5	+1	LSB
Nominal Resistor Tolerance	ΔR_{AB}	T_A = +25°C	−30		+30	%
Resistance Temperature Coefficient[3]	$(\Delta R_{AB}/R_{AB})/\Delta T*10^6$	$V_{AB} = V_{DD}$, wiper = no connect		−300		ppm/°C
Wiper Resistance	R_W	V_{DD}/V_{SS} = ±15 V		120	200	Ω
		V_{DD}/V_{SS} = ±5 V		260		Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE						
Integral Nonlinearity[4]	INL	V_{DD}/V_{SS} = ±15 V	−1	±0.5	+1	LSB
Differential Nonlinearity[4]	DNL	V_{DD}/V_{SS} = ±15 V	−1	±0.5	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T*10^6$	Code = 0x40		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0x7F, V_{DD}/V_{SS} = ±15 V	−3	−1.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00, V_{DD}/V_{SS} = ±15 V	0	+1.5	+3	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A, B, W}$		V_{SS}		V_{DD}	V
Capacitance[6] A, B	$C_{A, B}$	f = 1 MHz, measured to GND, code = 0x40		45		pF
Capacitance[6]	C_W	f = 1 MHz, measured to GND, code = 0x40		60		pF
Shut-down Supply Current[7]	I_{A_SD}	$V_A = V_{DD}$, V_B = 0 V, SHDN = 0		0.02	1	µA
Shut-down Wiper Resistance	R_{W_SD}	$V_A = V_{DD}$, V_B = 0 V, SHDN = 0, V_{DD} = +15 V		170	400	Ω
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_W$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V or 15 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V or 15 V			0.8	V
Output Logic High	V_{OH}	$R_{Pull-up}$ = 2.2 kΩ to 5 V	4.9			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = 5 V, V_{DD} = 15 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}/V_{SS}	Dual-supply range	±4.5		±16.5	V
Power Supply Range	V_{DD}	Single-supply range, V_{SS} = 0	4.5		33	V
Positive Supply Current	I_{DD}	V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±15 V			2	mA
		V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±5 V		12	25	µA
Negative Supply Current	I_{SS}	V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±15 V			−0.1	mA
		V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±5 V			−0.1	mA
Power Dissipation[8]	P_{DISS}	V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±15 V			31.5	mW
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD}/\Delta V_{SS}$ = ±15 V ±10%	−0.2	±0.05	+0.2	%/%
DYNAMIC CHARACTERISTICS[6, 9,10]						
Bandwidth −3 dB	BW	code = 0x40		470		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.006		%
V_W Settling Time	t_S	V_A = 10 V, V_B = 0 V, ±1 LSB error band		4		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 5 kΩ, f = 1 kHz		0.9		$nV\sqrt{Hz}$

ELECTRICAL CHARACTERISTICS—50 kΩ, 100 kΩ VERSIONS

V_{DD}/V_{SS} = ±15 V ± 10% or ±5 V ± 10%, $V_A = +V_{DD}$, $V_B = V_{SS}$/0 V, −40°C < T_A < +85°C, unless otherwise noted.

Table 2. (Editor, please delete notes 12-

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A = NC,	−1	±0.5	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A = NC, R_{AB} = 50 kΩ	−1.5	±0.5	+1.5	LSB
		R_{WB}, V_A = NC, R_{AB} = 100 kΩ	−1	±0.5	+1	LSB
Nominal Resistor Tolerance	ΔR_{AB}	T_A = +25°C	−30		+30	%
Resistance Temperature Coefficient[3]	$(\Delta R_{AB}/R_{AB})/\Delta T*10^6$	$V_{AB} = V_{DD}$, wiper = no connect		−300		ppm/°C
Wiper Resistance	R_W	V_{DD}/V_{SS} = ±15 V		120	200	Ω
		V_{DD}/V_{SS} = ±5 V		260		Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE						
Integral Nonlinearity[4]	INL		−1	±0.5	+1	LSB
Differential Nonlinearity[4]	DNL		−1	±0.5	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T*10^6$	Code = 0x40		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0x7F	−2	−0.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	+0.5	+1	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A, B, W}$		V_{SS}		V_{DD}	V
Capacitance[6] A, B	$C_{A, B}$	f = 1 MHz, measured to GND, code = 0x40		45		pF
Capacitance[6]	C_W	f = 1 MHz, measured to GND, code = 0x40		60		pF
Shut-down Supply Current[7]	I_{A_SD}	$V_A = V_{DD}$, V_B = 0 V, SHDN = 0		0.02	1	µA
Shut-down Wiper Resistance	R_{W_SD}	$V_A = V_{DD}$, V_B = 0 V, SHDN = 0, V_{DD} = +15 V		170	400	Ω
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_W$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V or 15 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V or 15 V			0.8	V
Output Logic High	V_{OH}	$R_{Pull-up}$ = 2.2 kΩ to 5 V	4.9			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = 5 V, V_{DD} = 15 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}/V_{SS}	Dual-supply range	±4.5		±16.5	V
Power Supply Range	V_{DD}	Single-supply range, V_{SS} = 0	4.5		33	V
Positive Supply Current	I_{DD}	V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±15 V			2	mA
		V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±5 V		12	25	µA
Negative Supply Current	I_{SS}	V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±15 V			−0.1	mA
		V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±5 V			−0.1	mA
Power Dissipation[8]	P_{DISS}	V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±15 V			31.5	mW
Power Supply Rejection Ratio	PSRR		−0.25	±0.1	+0.25	%/%
DYNAMIC CHARACTERISTICS[6,9,10]						
Bandwidth −3 dB	BW	R_{AB} = 50 kΩ, code = 0x40		90		kHz
		R_{AB} = 100 kΩ, code = 0x40		50		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.002		%
V_W Settling Time	t_S	V_A = 10 V, V_B = 0 V, ±1 LSB error band		4		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 25 kΩ, f = 1 kHz		2		$nV\sqrt{Hz}$

Table 3.

INTERFACE TIMING CHARACTERISTICS (Applies to All Parts)[6, 11]					
Clock Frequency	f_{CLK}			4	MHz
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock level high or low	120		ns
Data Setup Time	t_{DS}		30		ns
Data Hold Time	t_{DH}		20		ns
CLK to SDO Propagation Delay[12]	t_{PD}	$R_{Pull\text{-}up}$ = 2.2 kΩ, C_L < 20 pF	10	100	ns
$\overline{CS}$ Setup Time	t_{CSS}		120		ns
$\overline{CS}$ High Pulse Width	t_{CSW}		150		ns
Reset Pulse Width	t_{RS}		120		ns
CLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}		10		ns
CLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		120		ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		120		ns

[1] Typical represent average reading at +25°C, V_{DD} = +15 V, and V_{SS} = −15 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from an ideal value measured between successive tap positions. Parts are guaranteed monotonic.
[3] Pb-free parts have a 35 ppm/°C temperature coefficient.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output digital-to-analog converter. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminals A, B, and W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] Measured at the A terminal. A terminal is open circuit in shutdown mode.
[8] P_{DISS} is calculated from $(I_{DD} \times V_{DD})$+abs$(I_{SS} \times V_{SS})$. CMOS logic level inputs result in minimum power dissipation.
[9] Bandwidth, noise, and settling times are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.
[10] All dynamic characteristics use V_{DD} = +15 V and V_{SS} = −15 V.
[11] See Figure 3 for the location of the measured values. All input control voltages are specified with $t_R = t_F$ = 1 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. Switching characteristics are measured using V_{DD} = +15 V and V_{SS} = −15 V.
[12] Propagation delay depends on value of V_{DD}, $R_{Pull\text{-}up}$ and C_L.

3-WIRE DIGITAL INTERFACE

Table 4.AD7376 Serial Data-Word Format[1]

D6	D5	D4	D3	D2	D1	D0
MSB						LSB
2^6						2^0

[1] Data is loaded MSB first.

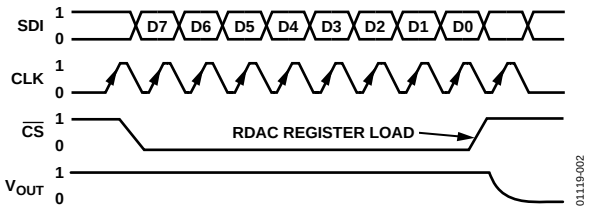

Figure 2. AD7376 3-Wire Digital Interface Timing Diagram
($V_A = V_{DD}$, $V_B = 0$ V, $V_W = V_{OUT}$)

(Illustrator, please delete one bit such that D7 and its associated CLK pulse are deleted)

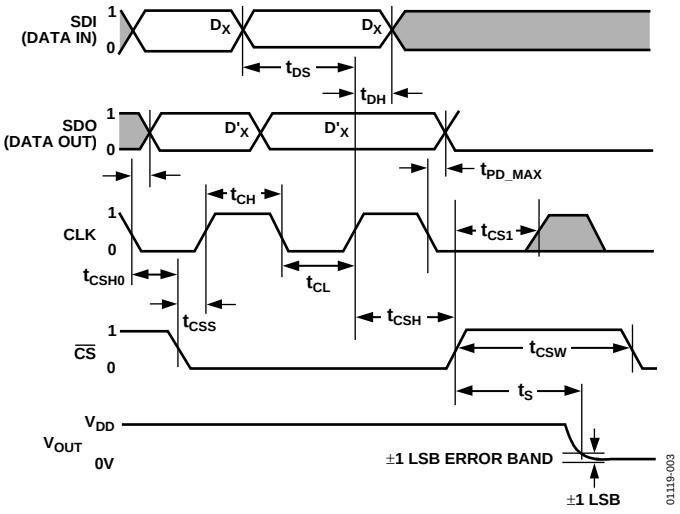

Figure 3. Detail Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V, +35 V
V_{SS} to GND	+0.3 V, −16.5 V
V_{DD} to V_{SS}	−0.3 V, +35 V
V_A, V_B, V_W to GND	V_{SS}, V_{DD}
Maximum Current	
I_{WB}, I_{WA} Pulsed	±20 mA
I_{WB} Continuous (R_{WB} ≤ 6 kΩ, A open, V_{DD}/V_{SS} = 30 V/0 V)[1]	±5 mA
I_{WA} Continuous (R_{WA} ≤ 6 kΩ, B open, V_{DD}/V_{SS} = 30 V/0 V)[1]	±5 mA
Digital Input and Output Voltages to GND	0 V, +7 V
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature (T_J MAX)[2]	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C
Package Power Dissipation	(T_J MAX − T_A)/θ_{JA}
Thermal Resistance θ_{JA}	
SOIC (SOL-16)	120°C/W
TSSOP-14	240°C/W

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Package power dissipation = (T_{JMAX} − T_A)/θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

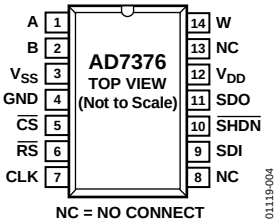

Figure 4. TSSOP-14 Pin Configuration

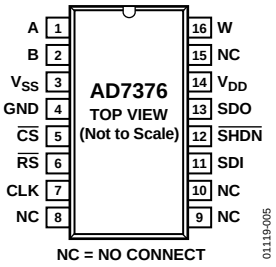

Figure 5. SOL-16 Pin Configuration

Table 6.Pin Function Descriptions

Pin No.			
TSSOP -14	**SOL-16**	**Mnemonic**	**Description**
1	1	A	A terminal. $V_{SS} \le V_A \le V_{DD}$.
2	2	B	B terminal. $V_{SS} \le V_B \le V_{DD}$.
3	3	V_{SS}	Negative Power Supply.
4	4	GND	Digital Ground.
5	5	$\overline{CS}$	Chip Select Input, active low. When $\overline{CS}$ returns high, data is loaded into the wiper register.
6	6	$\overline{RS}$	Reset to Midscale.
7	7	CLK	Serial Clock Input. Positive-edge triggered.
8	8, 9, 10	NC	No Connect. Let it float or ground.
9	11	SDI	Serial Data Input (data loads MSB first).
10	12	$\overline{SHDN}$	Shutdown. A terminal open ended; W and B terminals shorted. Can be used as programmable preset.
11	13	SDO	Serial Data Output.
12	14	V_{DD}	Positive Power Supply.
13	15	NC	No Connect. Let it float or ground.
14	16	W	Wiper Terminal. $V_{SS} \le V_W \le V_{DD}$.

TYPICAL PERFORMANCE CHARACTERISTICS

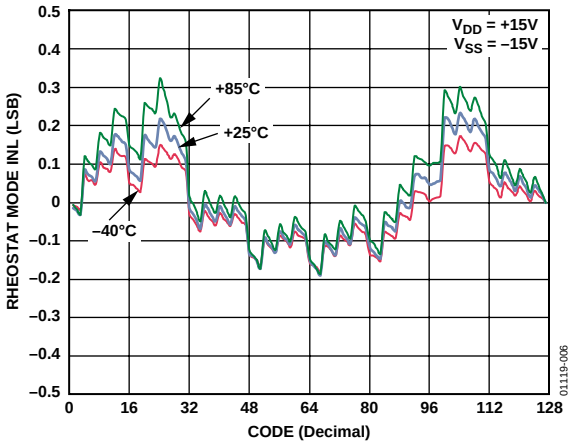

Figure 6. Resistance Step Position Nonlinearity Error vs. Code

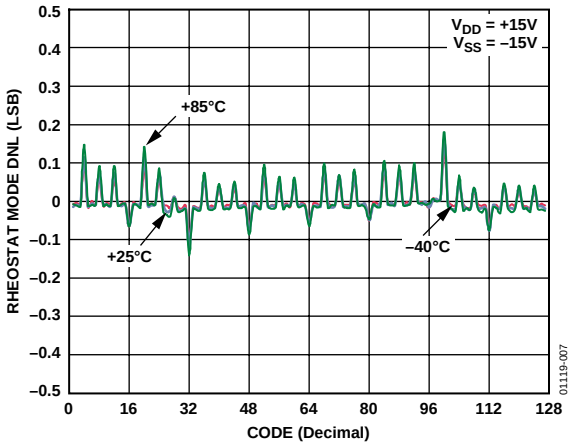

Figure 7. Relative Resistance Step Change from Ideal vs. Code

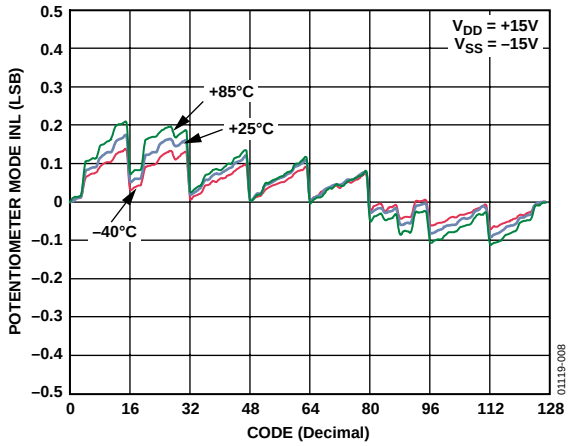

Figure 8. Potentiometer Divider Nonlinearity Error vs. Code

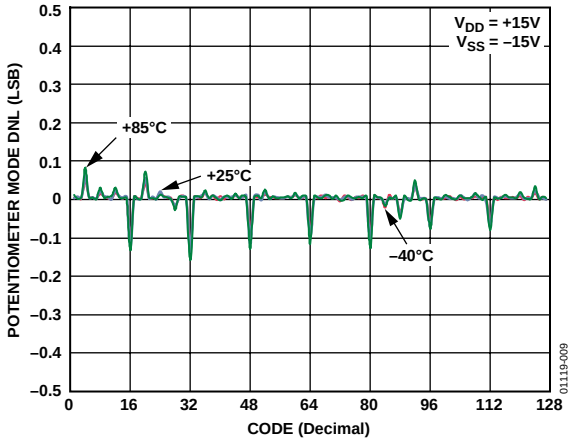

Figure 9. Potentiometer Divider Differential Nonlinearity Error vs. Code

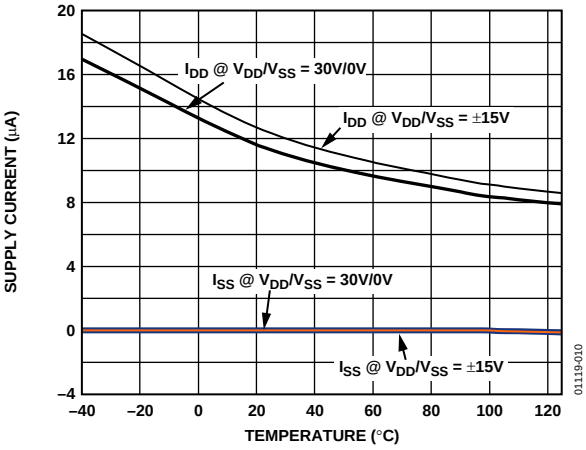

Figure 10. Supply Current (I_{DD}, I_{SS}) vs. Temperature

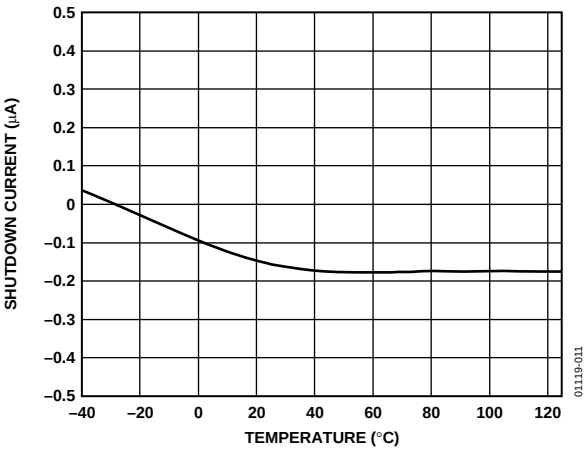

Figure 11. Shutdown Current vs. Temperature

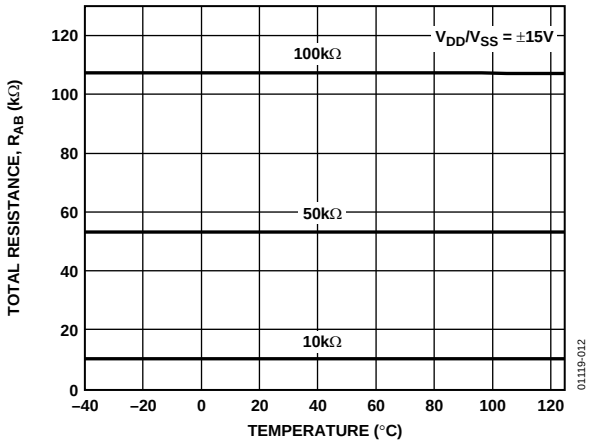

Figure 12. Total Resistance vs. Temperature

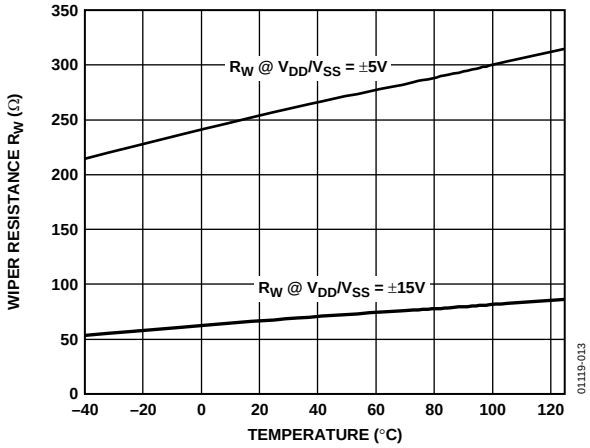

Figure 13. Wiper Contact Resistance vs. Temperature

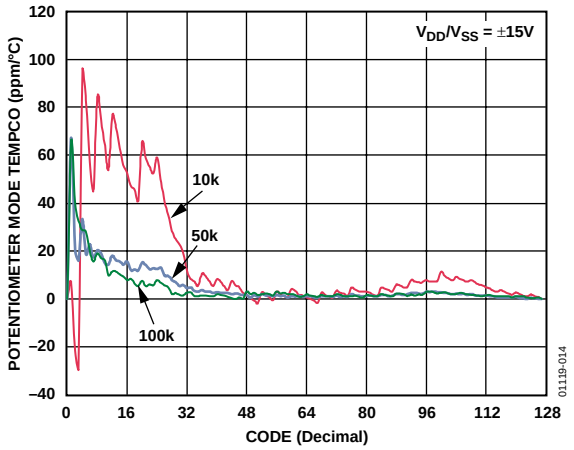

Figure 14. ($\Delta R_{WB}/R_{WB}$)/ΔT Rheostat Mode Tempco

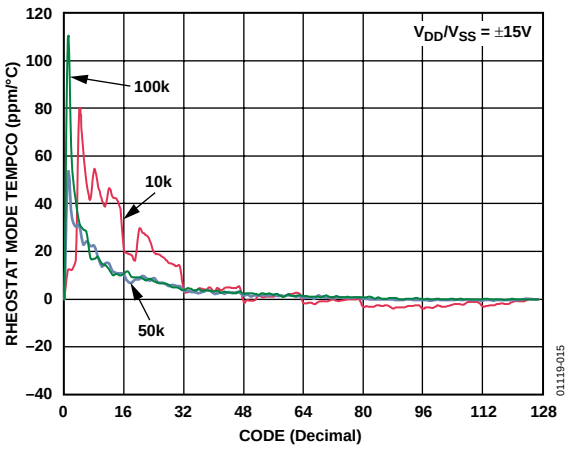

Figure 15. ($\Delta V_{WB}/V_{WB}$)/ΔT Potentiometer Mode Tempco

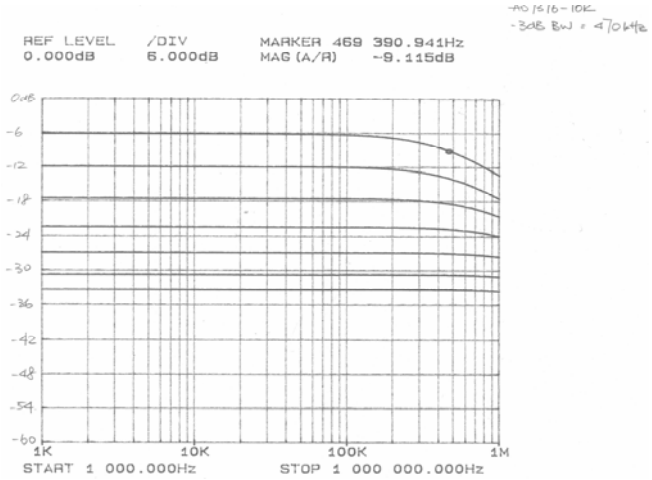

Figure 16. 10 kΩ Gain vs. Frequency vs. Code

(Jim, please label 0x40, 0x20, 0x10, 0x08, 0x04, 0x02, 0x01 from top to bottom)

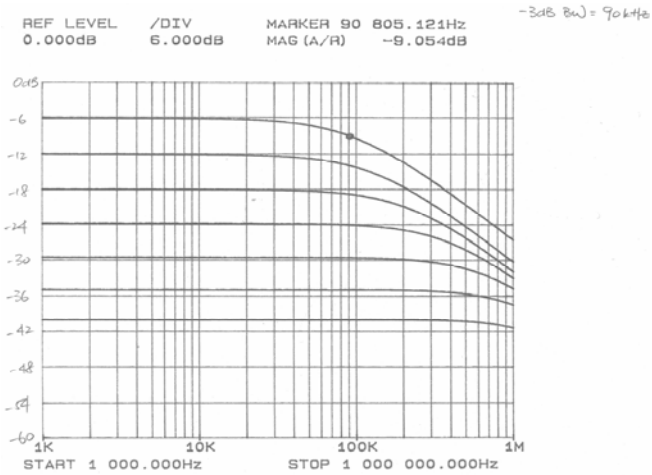

Figure 17. 50 kΩ Gain vs. Frequency vs. Code

(Jim, please label 0x40, 0x20, 0x10, 0x08, 0x04, 0x02, 0x01 from top to bottom)

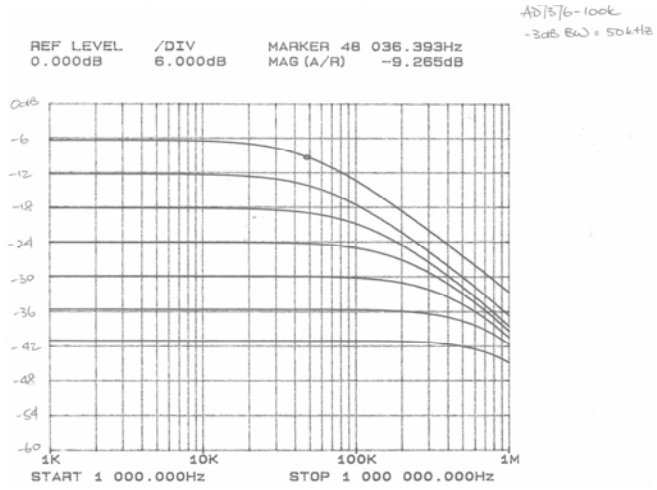

Figure 18. 100 kΩ Gain vs. Frequency vs. Code

(Jim, please label 0x40, 0x20, 0x10, 0x08, 0x04, 0x02, 0x01 from top to bottom)

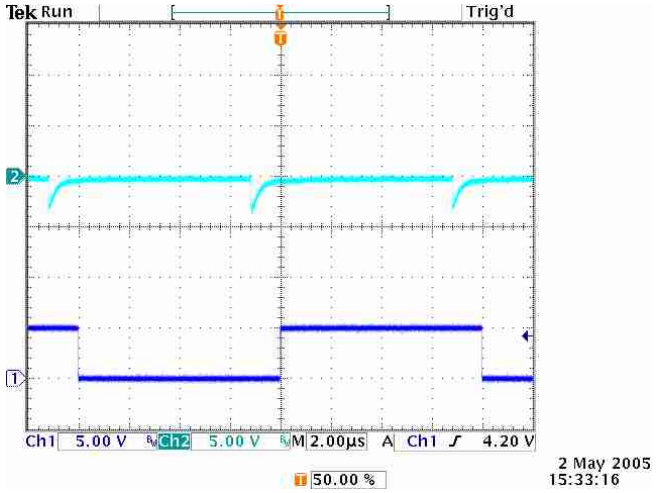

Figure 19. Midscale to Midscale-1 Transition Glitch

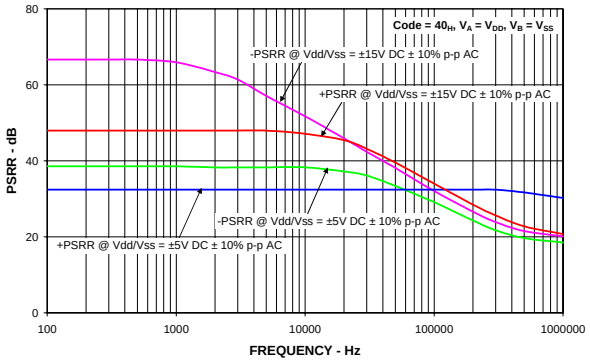

Figure 20. Power Supply Rejection vs. Frequency

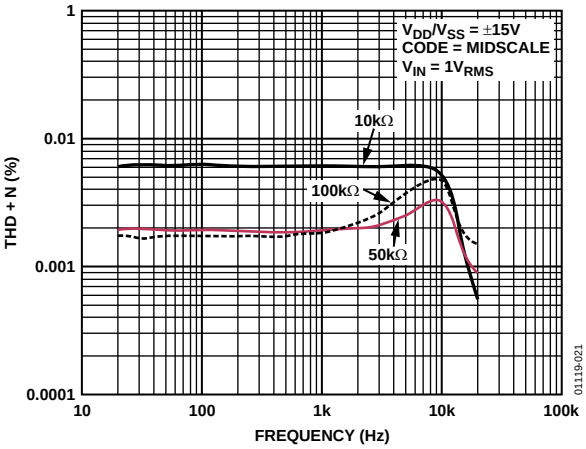

Figure 21. Total Harmonic Distortion Plus Noise vs. Frequency

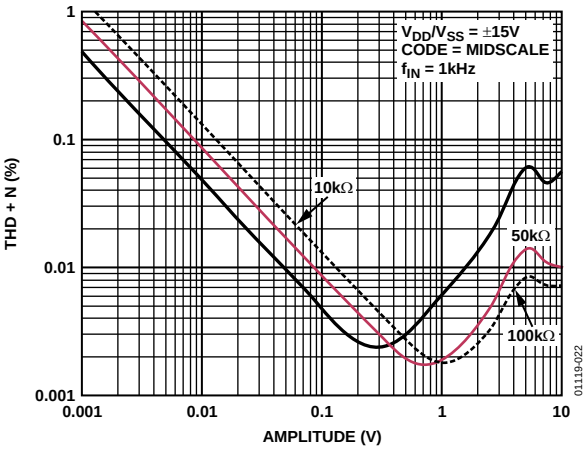

Figure 22

Figure 23. Total Harmonic Distortion Plus Noise vs. Amplitude

(Illustrator, please point 10kΩ to the solid black curve)

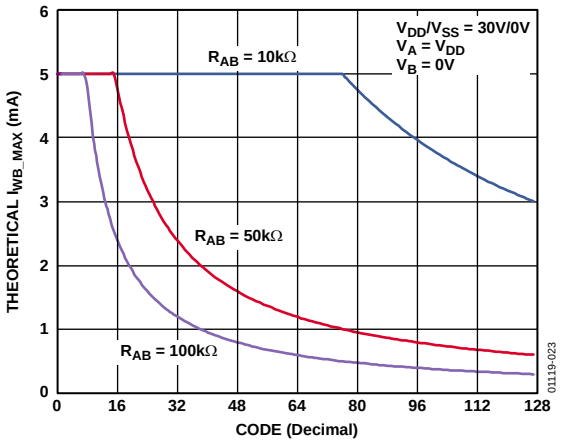

Figure 24

Figure 25. Theoretical Maximum Current vs. Code

THEORY OF OPERATION

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

When only two terminals are used, for example, R_{WA} or R_{WB} as shown in Figure 24, the part operates in rheostat mode. The nominal resistance between Terminals A and B, R_{AB}, is available in 10 kΩ, 50 kΩ, and 100 kΩ and has 128 tap points accessed by the wiper terminal. The 7-bit data in the RDAC latch is decoded to select one of the 128 possible settings (see Figure 27).

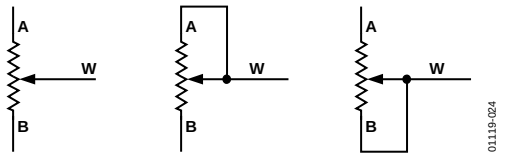

Figure 26. Rheostat Mode Configuration

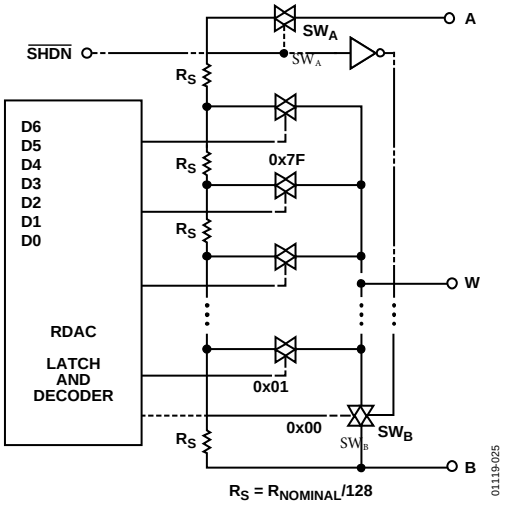

Figure 27. AD7376 Equivalent RDAC Circuit

The general equation determining the digitally programmed output resistance between the W and the B terminals is

$$R_{WB}(D) = \frac{D}{128} \times R_{AB} + R_W \qquad (1)$$

where:
D is the decimal equivalent of the binary code loaded in the 7-bit RDAC register from 0 to 127.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the on resistance of the internal switch.

The AD7376 wiper switches are designed with the transmission gate CMOS topology with the gate voltage derived from the V_{DD}. The switch's on resistance, R_W, is not only a function of V_{DD} but also of temperature, see Figure 13. The AD7376 switch's on resistance is insensitive to the tap point potential and remains relatively flat at 120 Ω typical at V_{DD} of 15 V and the temperature of 25°C.

Assuming that a 10 kΩ part is used, the wiper's first connection starts at the B terminal for programming code of 0x00, where SW_B is closed. The minimum resistance between Terminals W and B is therefore 120 Ω in general. The second connection is the first tap point, which corresponds to 198 Ω (R_{WB} = 1/128* R_{AB} + R_W = 78 Ω + 120 Ω) for programming code of 0x01 and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,042 Ω (R_{AB} – 1 LSB + R_W). Note that in the zero-scale condition, a finite wiper resistance of 120 Ω is present. Care should be taken to limit the current conducted between the W and B Terminals in this state to a maximum pulse current of 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the W and A Terminals also produces a digitally controlled complementary resistance, R_{WA}. When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded into the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{128 - D}{128} \times R_{AB} + R_W \qquad (2)$$

Typical device-to-device matching is process-lot dependent and may vary by up to ±30%.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at Wiper W to Terminal B and Wiper W to Terminal A that is proportional to the input voltage at Terminal A to Terminal B. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across Terminal A to Terminal B, Wiper W to Terminal A, and Wiper W to Terminal B can be at either polarity.

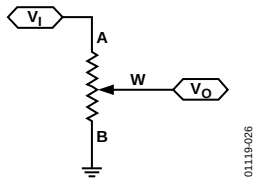

Figure 28. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for the purpose of approximation, connecting the A terminal to 30 V and the B terminal to ground produces an output voltage at the Wiper W to Terminal B ranging from 0 V to 1 LSB less than 30 V. Each LSB of voltage is equal to the voltage applied across Terminals A and B divided by the 128 positions of the potentiometer divider. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to Terminals A and B is

$$V_W(D) = \frac{D}{128} V_A \qquad (3)$$

A more accurate calculation, which includes the effect of wiper resistance, V_W is

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} V_A + \frac{R_{WA}(D)}{R_{AB}} V_B \qquad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike when in rheostat mode, the output voltage in divider mode is primarily dependent on the ratio, not the absolute values, of the internal resistors R_{WA} and R_{WB}. Therefore, the temperature drift reduces to 5 ppm/°C.

3-WIRE SERIAL BUS DIGITAL INTERFACE

The AD7376 contains a 3-wire digital interface ($\overline{CS}$, CLK, and SDI). The 7-bit serial word must be loaded MSB first. The format of the word is shown in Figure 2. The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. When $\overline{CS}$ is high, the clock loads data into the serial register upon each positive clock edge.

The data setup and hold times in the specifications table determine the valid timing requirements. The AD7376 uses a 7-bit serial input data register word that is transferred to the internal RDAC register when the $\overline{CS}$ line returns to logic high. Extra MSB bits are ignored.

When the reset ($\overline{RS}$) pin is asserted, the wiper resets to the midscale value.

When the $\overline{SHDN}$ pin is asserted, the AD7376 opens SW_A to let the A terminal float and to short Wiper W to Terminal B. The AD7376 consumes negligible power during the shutdown mode and resumes the previous setting once the $\overline{SHDN}$ pin is released. On the other hand, the AD7376 can be programmed with any settings during shutdown. With an extra programmable I/O asserts shutdown during power up, this unique feature allows the AD7376 with programmable preset at any desirable level.

Table 7 shows the logic truth table of all operation.

Table 2.Input Logic Control Truth Table[1]

CLK	$\overline{CS}$	$\overline{RS}$	$\overline{SHDN}$	Register Activity
L	L	H	H	Enables SR, enables SDO pin.
P	L	H	H	Shifts one bit in from the SDI pin. The seventh previously entered bit is shifted out of the SDO pin.
X	P	H	H	Loads SR data into 7-bit RDAC latch.
X	H	H	H	No operation.
X	X	L	H	Sets 7-bit RDAC latch to midscale, wiper centered, and SDO latch cleared.
X	H	P	H	Latches 7-bit RDAC latch to 0x40.
X	H	H	L	Opens circuits resistor of Terminal A, connects Wiper W to Terminal B, turns off SDO output transistor.

[1] P = positive edge, X = don't care, SR = shift register.

DAISY-CHAIN OPERATION

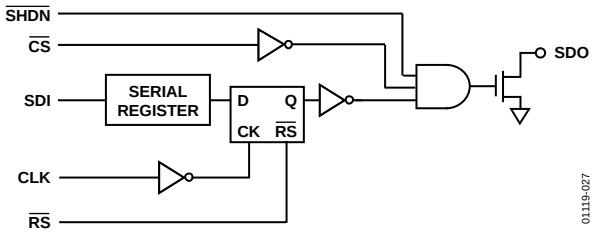

Figure 29. Detail SDO Output Schematic of the AD7376

Figure 29 shows the details of the serial data output pin (SDO). SDO shifts out the SDI content in the previous frame; therefore, it can be used for daisy-chain multiple devices. The SDO pin contains an open-drain N-Channel MOSFET and requires a pull-up resistor if the SDO function is used. Users need to tie the SDO pin of one package to the SDI pin of the next package. For example, in Figure 30 if two AD7376s are daisy-chained, a total of 14 bits of data are required for each operation. The first set of seven bits goes to U2; the second set of seven bits goes to U1. $\overline{CS}$ should be kept low until all 14 bits are clocked into their respective serial registers. Then $\overline{CS}$ is pulled high to complete the operation. When daisy chain multiple devices, users may need to increase the clock period because the pull-up resistor and the capacitive loading at the SDO-SDI interface may induce a time delay to subsequent devices.

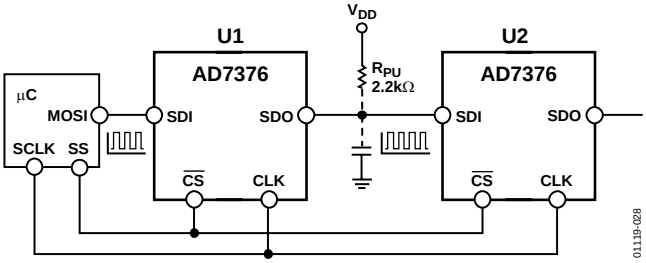

Figure 30. Daisy-Chain Configuration

ESD PROTECTION

All digital inputs are protected with a series input resistor and a Zener ESD structure shown in Figure 31. These structures apply to digital input pins $\overline{CS}$, CLK, SDI, SDO, $\overline{RS}$, and $\overline{SHDN}$

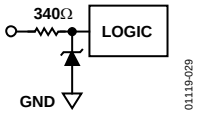

Figure 31. Equivalent ESD Protection Circuit

All analog terminals are also protected by Zener ESD protection diodes, as shown in Figure 32.

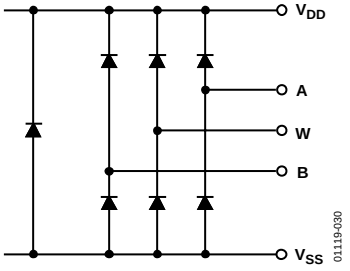

Figure 32. Equivalent ESD Protection Analog Pins

TERMINAL VOLTAGE OPERATING RANGE

The AD7376 V_{DD} and V_{SS} power supplies define the boundary conditions for proper 3-terminal digital potentiometer operation. Applied signals present on Terminals A, B, and W that are more positive than V_{DD} or more negative than V_{SS} will be clamped by the internal forward-biased diodes (see Figure 32).

POWER-UP AND POWER-DOWN SEQUENCES

Because of the ESD protection diodes that limit the voltage compliance at Terminals A, B, and W (see Figure 32), it is important to power V_{DD}/V_{SS} before applying voltage to Terminals A, B, and W. Otherwise, the diodes are forward-biased such that V_{DD}/V_{SS} are powered unintentionally and affect the system. Similarly, V_{DD}/V_{SS} should be powered down last. The ideal power-up sequence is in the following order: GND, V_{DD}, V_{SS}, digital inputs, and $V_A/V_B/V_W$. The order of powering V_A, V_B, V_W, and the digital inputs is not important, as long as they are powered after V_{DD}/V_{SS}.

LAYOUT AND POWER SUPPLY BIASING

It is a good practice to employ a compact, minimum lead-length layout design. The leads to the input should be as direct as possible, with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors. Low ESR (equivalent series resistance) 1 µF to 10 µF tantalum or electrolytic capacitors should be applied at the supplies to minimize transient disturbances and filter low frequency ripple. Figure 33 illustrates the basic supply bypassing configuration for the AD7376.

The ground pin of the AD7376 is a digital ground reference. To minimize the digital ground bounce, the AD7376 digital ground terminal should be joined remotely to the analog ground (see Figure 33).

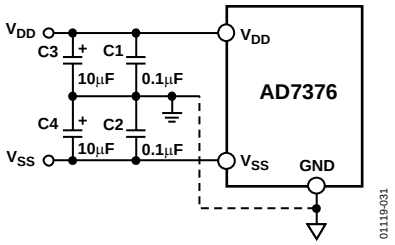

Figure 33. Power Supply Bypassing

APPLICATIONS

HIGH VOLTAGE DAC

AD7376 can be configured as a high voltage DAC as high as 30V. The circuit is shown in Figure 32. The output is

$$V_O(D) = \frac{D}{128}[1.2\ \text{V} \times (1 + \frac{R_2}{R_1})] \qquad (5)$$

Where *D* is the decimal code from 0 to 127.

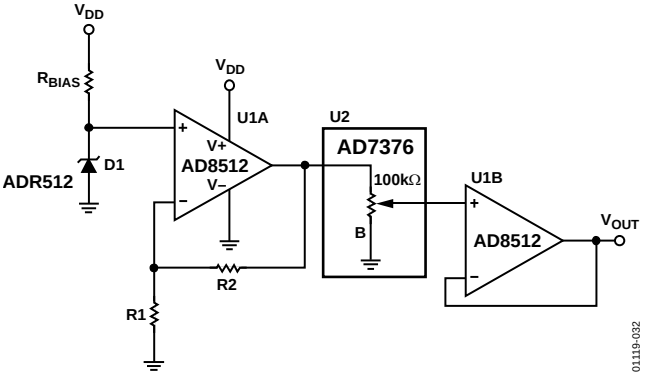

Figure 34. High Voltage DAC

PROGRAMMABLE POWER SUPPLY

With a boost regulator such as ADP1611, AD7376 can be used as the variable resistor at the regulator's FB pin to provide the programmable power supply (see Figure 35). The output is

$$V_O = 1.23\ \text{V} \times (1 + \frac{(D/128) \cdot R_{AB}}{R_2}] \qquad (6)$$

Note that the AD7376's V_{DD} is derived from the output. Initially L1 acts as a short, and V_{DD} is one diode voltage drop below +5 V. The output slowly establishes to the final value.

The AD7376 shutdown sleep-mode programming can be used to program a desirable preset level at power up.

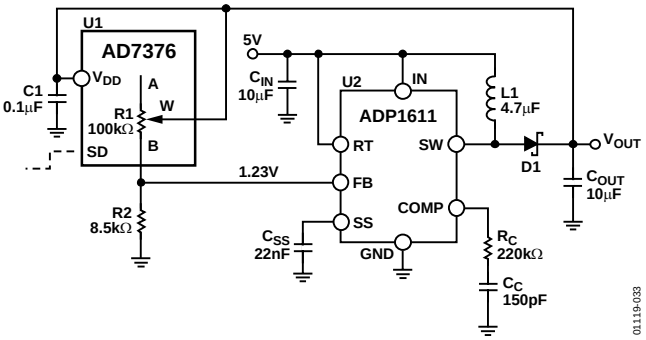

Figure 35. Programmable Power Supply

AUDIO VOLUME CONTROL

Because of its good THD performance and high voltage capability, AD7376 can be used as a digital volume control. If AD7376 is used directly as an audio attenuator or gain amplifier, a large step change in the volume level at any arbitrary time can lead to an abrupt discontinuity of the audio signal, causing an audible zipper noise. To prevent this, a zero-crossing window detector can be inserted to the $\overline{CS}$ line to delay the device update until the audio signal crosses the window. Since the input signal can operate on top of any DC levels rather than absolute zero volt level, thus zero-crossing in this case means the signal is AC coupled and the DC offset level is the signal zero reference point. The configuration to reduce zipper noise and the result of using this configuration are shown in Figure 36 and Figure 37, respectively. The input is AC coupled by C1 (Illustrator, please change C6 to C1) and attenuated down before feeding into the window comparator formed by U_2, U_3, and U_{4B}. U_6 is used to establish the signal zero reference. The upper limit of the comparator is set above its offset and, therefore, the output pulses high whenever the input falls between 2.502V and 2.497V (or 0.005V window) in this example. This output is AND'ed with the chip select signal such that the AD7376 updates whenever the signal crosses the window. To avoid constant update of the device, the chip select signal should be programmed as two pulses, rather than the one shown in Figure 2.

In Figure 37, the lower trace shows that the volume level changes from a quarter scale to full scale when a signal change occurs near the zero-crossing window.

The AD7376 shutdown sleep-mode programming feature can be used to mute the device at power up.

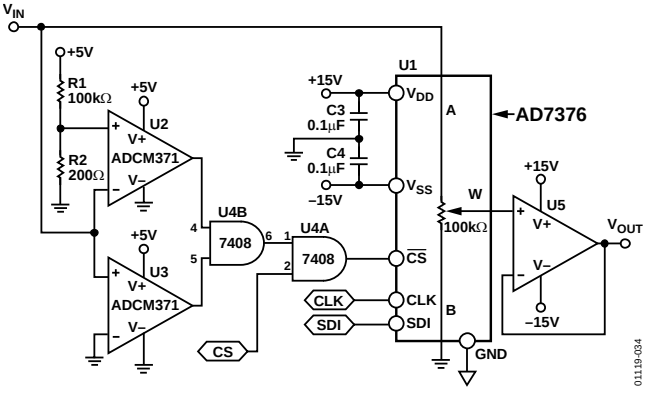

Figure 36. Audio Volume Control with Zipper Noise Reduction

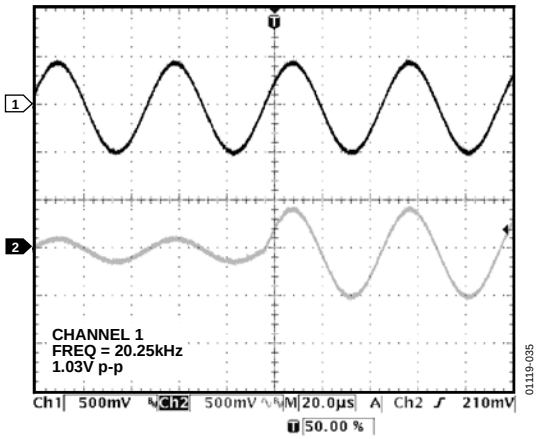

Figure 37. Input(trace 1) and Output (trace 2) of the Circuit inFigure 36. The lower trace shows that the volume level changes from a quarter scale to full scale with change occurs near zero crossing window

OUTLINE DIMENSIONS

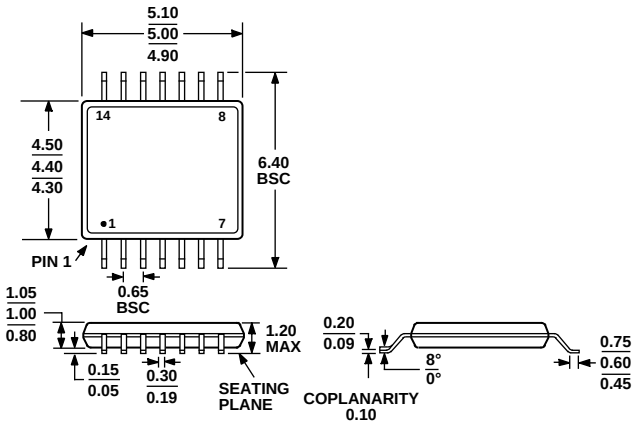

Figure 38. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

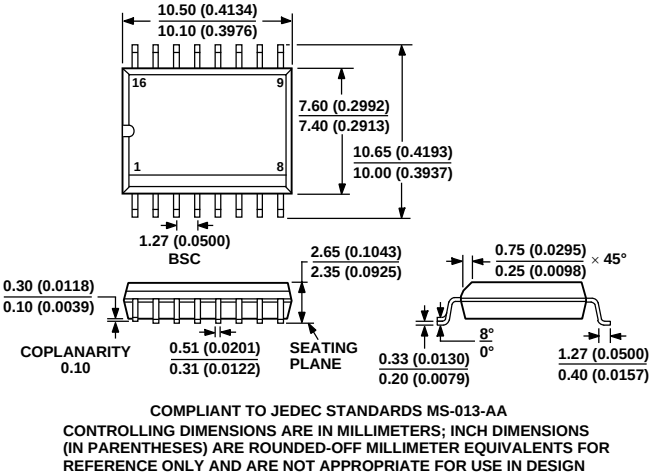

Figure 39. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	kΩ	Temperature Range	Package Description	Package Options	Quantity	Branding[1,2]
AD7376AR10	10	−40°C to +85°C	16-Lead SOIC_W	R-16	47	A10
AD7376AR10-REEL	10	−40°C to +85°C	16-Lead SOIC_W	R-16	1,000	A10
AD7376ARU10	10	−40°C to +85°C	14-Lead TSSOP	RU-14	96	A10
AD7376ARU10-REEL7	10	−40°C to +85°C	14-Lead TSSOP	RU-14	1,000	A10
AD7376ARUZ10 [3]	10	−40°C to +85°C	14-Lead TSSOP	RU-14	96	A10#
AD7376ARUZ10-R7 [3]	10	−40°C to +85°C	14-Lead TSSOP	RU-14	1,000	A10#
AD7376ARWZ10 [3]	10	−40°C to +85°C	16-Lead SOIC_W	RW-16	47	A10#
AD7376ARWZ10-RL[3]	10	−40°C to +85°C	16-Lead SOIC_W	RW-16	1,000	A10#
AD7376AR50	50	−40°C to +85°C	16-Lead SOIC_W	R-16	47	A50
AD7376AR50-REEL	50	−40°C to +85°C	16-Lead SOIC_W	R-16	1,000	A50
AD7376ARU50	50	−40°C to +85°C	14-Lead TSSOP	RU-14	96	A50
AD7376ARU50-REEL7	50	−40°C to +85°C	14-Lead TSSOP	RU-14	1,000	A50
AD7376ARUZ50 [3]	50	−40°C to +85°C	14-Lead TSSOP	RU-14	96	A50#
AD7376ARWZ50 [3]	50	−40°C to +85°C	16-Lead SOIC_W	RW-16	47	A50#
AD7376ARUZ100 [3]	100	−40°C to +85°C	14-Lead TSSOP	RU-14	96	A100#
AD7376ARUZ100-R7 [3]	100	−40°C to +85°C	14-Lead TSSOP	RU-14	1,000	A100#
AD7376ARWZ100 [3]	100	−40°C to +85°C	16-Lead SOIC_W	RW-16	47	A100#
AD7376EVAL	10				1	

1. In SOICWB-16 package top marking, Line 1 shows AD7376; Line 2 shows the branding information, such that A10 = 10 kΩ, A50 = 50 kΩ, and A100 = 100 kΩ; Line 3 shows the date code in YYWW; Line 4 shows the lot number. In TSSOP-14 package top marking, Line 1 shows 7376; Line 2 shows the branding information, such that A10 = 10 kΩ, A50 = 50 kΩ, and A100 = 100 kΩ; Line 3 shows the date code in YWW; Back side shows the lot number.
2. In TSSOP-14 package top marking, Line 1 shows 7376; Line 2 shows the branding information, such that A10 = 10 kΩ, A50 = 50 kΩ, and A100 = 100 kΩ; Line 3 shows the date code in YWW; Back side shows the lot number.
3. Z = Pb-free part

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